PATENT

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IN THE CLAIMS:

Please find below a listing of all of the pending claims. The status of each claim is set forth in parentheses.

1. (Currently Amended) A method of forming an integrated circuit comprising the steps of:

forming a circuit function block on an IC chip; and

~~forming a decoupling capacitor in an area above the circuit function block;~~

forming an inter-digitated capacitance structure in an area above the circuit function block, wherein forming the inter-digitated capacitance structure comprises forming a plurality of inter-digitated metal fingers extending outward from at least one inter-digitated metal;

forming a top metal layer;

forming a bottom metal layer;

forming a dielectric material, wherein the dielectric material is deposited between the plurality of inter-digitated metal fingers; and

forming a plurality of de-coupling capacitances between the inter-digitated capacitance structure, the top metal layer and bottom metal layer, and the dielectric material.

2-3. (Cancelled)

4. (Original) The method of claim 3, wherein the step of forming a dielectric material further comprises the step of:

forming a first dielectric layer below the inter-digitated metal fingers and the bottom metal layer, wherein the first dielectric layer has a predetermined thickness.

5. (Original) The method of claim 4, wherein the first dielectric layer is a low dielectric material.

6. (Original) The method of claim 3, wherein the step of forming an inter-digitated capacitance structure further comprising the step of:

forming a second dielectric layer between the inter-digitated metal fingers and the top metal layer.

7. (Original) The method of claim 6, wherein the second dielectric layer comprises a predetermined dielectric material.

8. (Original) The method of claim 3, wherein the first metal layer is a plate which isolates the de-coupling capacitor from the circuit block.

9. (Original) The method of claim 2, wherein the step of forming an inter-digitated capacitance structure further comprising the steps of:

forming a inter-layer dielectric layer below the bottom metal layer.

10. (Cancelled)

11. (Currently Amended) A method of forming an integrated circuit comprising the steps of:

forming a circuit function block on an IC chip;

forming a first metal layer separating a decoupling capacitor circuit from the circuit function block; ~~and~~

forming a second metal layer; and

forming an inter-digitated capacitance structure on the first metal layer, wherein the inter-digitated capacitance structure is etched to form a predetermined pattern of inter-digitated metal fingers, wherein forming the inter-digitated capacitance structure further comprises forming a plurality of de-coupling capacitances between the inter-digitated capacitance structure, the first metal layer and the second metal layer.

12. (Original) The method of claim 11, wherein the inter-digitated capacitance structure comprises the steps of:

forming at least one inter-digitated metal finger; and

forming a dielectric layer is deposited between the at least one inter-digitated metal finger.

13. (Original) The method of claim 11, the step of forming an integrated circuit further comprising the step of:

forming a first dielectric layer above the circuit function block and the inter-digitated capacitance structure, such that the first dielectric layer has a predetermined thickness.

14. (Original) The method of claim 13, wherein the first dielectric material is a low dielectric material.

15. (Original) The method of claim 11, further comprising the steps of:

forming a second dielectric layer above the bottom metal plate.

16. (Currently Amended) An integrated circuit comprising:

a circuit function block having a predetermined circuit layout; and

an inter-digitated capacitance structure comprising at least one metal plate and a plurality of inter-digitated metal fingers on top of the circuit function block, wherein a plurality of de-coupling capacitances are formed between the inter-digitated capacitance structure, a first metal layer, and a second metal layer.

17. (Cancelled)

18. (Original) The integrated circuit of claim 16, further comprising:

a first dielectric layer formed on the circuit function block;

a third dielectric layer formed on the second metal layer; and

a third metal plate formed on the third dielectric layer.

19. (Original) The integrated circuit of claim 16, further comprising:

a second dielectric layer formed on top of the first metal layer.

20. (Original) The integrated circuit of claim 16, wherein the inter-digitated metal fingers extend from the metal plate in such a manner that the plurality of inter-digitated metal fingers are in parallel and have a predetermined separation and width.

21. (New) The integrated circuit of claim 1, wherein the inter-digitated capacitance structure is formed above a cache memory.

22. (New) The integrated circuit of claim 11, wherein the inter-digitated capacitance structure is formed above a cache memory.

23. (New) The integrated circuit of claim 16, wherein the inter-digitated capacitance structure is formed above a cache memory.